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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/663,977	09/17/2003	Hirohisa Tanabe	031794-3	1949

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EXAMINER	
YANCHUS III, PAUL B	

ART UNIT	PAPER NUMBER
2116	

MAIL DATE	DELIVERY MODE
05/14/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/663,977	TANABE ET AL.	
	Examiner	Art Unit	
	Paul B. Yanchus	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 21 February 2007.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 4-9 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 4-9 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This non-final office action is in response to the RCE filed on 2/21/07.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art [AAPA], in view of Kim, US Patent no. 6,845,454.

Regarding claim 4, AAPA discloses an interface circuit provided for each of a first device set as a master side and a second device set as a slave side [two peripheral devices], for performing a serial data transmission between the first and second devices on the basis of a control signal [VBUS] which is output from the master side [page 1], comprising:

an oscillation circuit which generates a first clock signal for data transmission [master oscillator, page 2];

a detection portion which monitors the control signal output a detection signal when there is a change in the control signal [detection circuit, page 2].

a process control portion which generates a clock-control signal [page 2]; and

a transmission function portion which performs a serial data transmission with the other device on the basis of the first clock signal [page 2]; and

stopping operation of the transmission function portion when the control signal indicates that there is no requirement to execute a transmission [page 2].

AAPA discloses using a master oscillator to generate both a first high frequency clock signal and a frequency divided low frequency clock signal for signal detection while in a low power mode [pages 2 and 3]. Consequently, AAPA does not disclose disabling a master oscillator when in a low power mode. Kim teaches using a first master [high frequency] clock generator for generating a high frequency clock signal for use in a normal power mode and a second low frequency clock generator for generating a low frequency clock signal in a low power mode instead of using a single high frequency for generating both of the high and low frequency clock signals. The master [high frequency] clock generator is disabled when the system is in a low power mode [column 1, line 40 – column 2, line 23]. It would have been obvious to one of ordinary skill in the art to apply the Kim teachings to the AAPA interface circuit. Disabling a high frequency clock generator and using a separate low frequency clock generator for generating a low frequency clock signal in a reduced power mode reduces power consumption of the interface circuit [Kim, column 1, lines 57-61].

Regarding claims 5-7, AAPA, as described above, discloses a detection portion, which monitors the control signal to output a detection signal when there is a change in the detection signal. AAPA is silent as to the specific components that are inside the detection portion.

Applicant(s) numerous definitions of the internal circuitry of the detection portion (claims 5-7) is construed to be an admission that the criticality does not reside in the type of internal circuitry utilized in the detection portion and hence are obvious variations of one another.

Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art [AAPA] and Kim, US Patent no. 6,845,454, in view of Dehghan, US Patent no. 6,275,087.

AAPA, as described above, discloses a detection portion, which monitors the control signal to output a detection signal when there is a change in the detection signal. AAPA is silent as to the specific components that are inside the detection portion. AAPA is silent as to the specific components that are inside the detection portion and therefore do not explicitly disclose a noise removal circuit for removing noise components from the control signal. However, as shown by Dehghan [column 6, lines 40-52], using noise removal circuitry in signal detection circuits is well known in the art. It would have been obvious to one of ordinary skill in the art to use well known noise removal circuitry in the AAPA detection portion of the interface circuit.

Response to Arguments

Applicant's arguments with respect to claims 4-9 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul B. Yanchus whose telephone number is (571) 272-3678. The examiner can normally be reached on Mon-Thurs 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on (571) 272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Paul Yanchus
May 8, 2007